CMP-based Gate-Last High-K Integration

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Ever increasing gate leakages through ultra-scaled SiO_2 gate dielectrics have led to extensive investigation of alternative materials with higher dielectric permittivity (high-K) in order to extend the unprecedented growth of IC complexity of the last four decades into the future.

However, high temperature annealing and aggressive RIE was found to degrade the initial quality of the sensitive high-K gate stack [1]. In order to minimize process induced oxide damage, we have integrated high-K dielectrics into a “gentle” damascene metal gate technology by means of chemical mechanical planarization (CMP) [2].

The major process steps are shown in Fig. 1. Initially, dummy gate stacks are formed conventionally including a self-aligned S/D ion implantation (Fig. 2). After PECVD oxide deposition and 1000°C RTA anneal the oxide is planarized by CMP down to the gate level and the dummy gates are removed completely by wet chemical etching, leaving a self-aligned imprint of the gate stack on the Si-wafer. Subsequently, the high-k gate dielectric is grown by MBE (crystalline Gd_2O_3 layers of 5.3 nm and 13.5 nm physical thickness) or evaporated (HfO_2 layers with 3.0 nm physical thickness and 0.8 nm SiO_2 interfacial layer). In addition, wafers with conventional SiO_2 are fabricated as a reference. Tungsten is deposited on top of the gate dielectrics and CMP is used to pattern the damascene metal gates. Standard back-end processing completes the fabrication.

The fabricated long-channel devices are fully functional (L>4µm). Typical output characteristics are shown for HfO_2-MOSFETs (Fig. 4) and Gd_2O_3-MOSFETs (Fig. 5).

Current work includes scaling down the process to the 100 nm regime. We have successfully structured dummy gates on SOI-substrates by means of e-beam lithography (Fig 2b) and we expect functional devices with high-K metal gate stack soon.

For the first time, we have successfully integrated novel high-K gate dielectrics with EOT down to 1.9 nm in a damascene metal gate process. Since the harsh processing is done prior to high-K deposition, PIOD-effects are minimized and the initial material quality of the crystalline high-K gate dielectric is largely preserved.

As a universal platform, the replacement gate technology provides the possibility of investigations of various gate dielectrics, metal gate materials and substrates and their combinations directly at the device level.

REFERENCES

[1] U. Schwalke, et al., Proc. ESSDERC, p.247 (2003).
[2] R. Endres, et. al., Microelectronic Reliability, **47**, pp. 528 – 531, (2007)

FIGURES

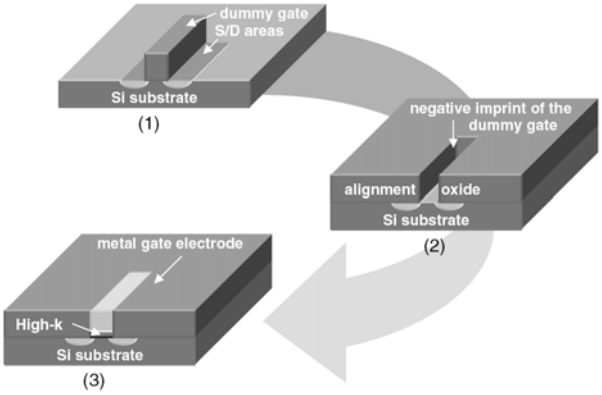

Fig. 1: Main process modules of the replacement gate technology.

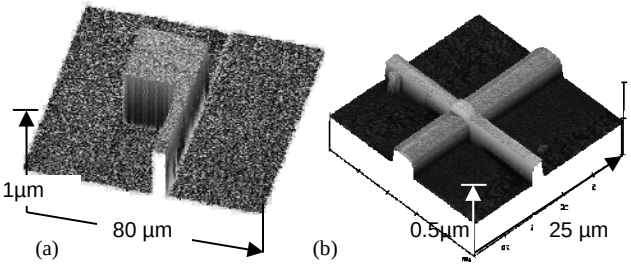

Fig. 2: Atomic force microscopy (AFM) image of a dummy gate structures produced with light optical lithography (a) and electron beam lithography (b).

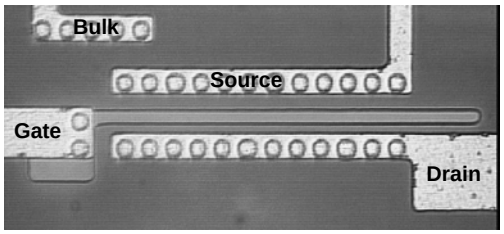

Fig. 3: nMOSFET with high-K Gd_2O_3 gate dielectric and tungsten gate electrode realized with the replacement gate process (gate length L= 4 µm and gate width W= 100 µm).

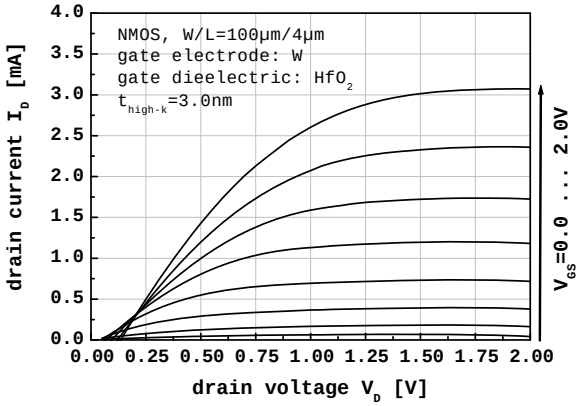

Fig. 4: Output characteristics of damascene metal gate HfO_2 nMOSFET.

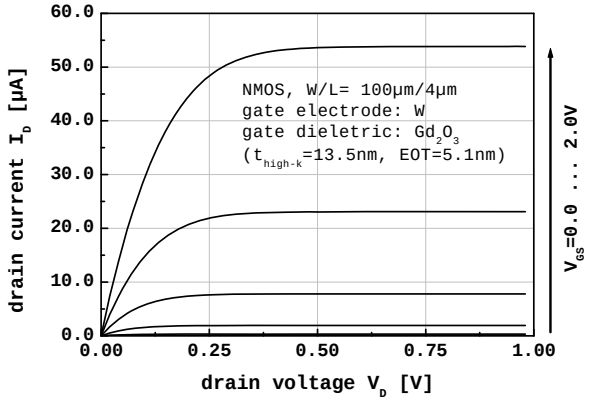

Fig. 5: Output characteristics of damascene metal gate Gd_2O_3 nMOSFET.