IEEE INTERNATIONAL CONFERENCE ON

DESIGN & TECHNOLOGY OF INTEGRATED SYSTEMS

IN NANOSCALE ERA

IEEE DTIS08 Booklet

March 26-28, 2008 Tozeur, TUNISIA

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IEEE Catalog Number: CFP0893A-PRT
ISBN: 978-1-4244-1576-2
Library of Congress: 2007905453
March 2008

ORGANIZED BY:

National Engineering School of Sfax (ENIS)

SUPPORTED BY:

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- **University of Montpellier II**
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Welcome to the IEEE DTIS'08 Conference

Welcome to the 3rd edition of the IEEE International Conference on Design & Technology of Integrated Systems in nanoscale era, IEEE DTIS'08.

The first edition was held in Guammarth (Tunisia) in September 2006 and the second edition in Rabat (Morocco) in September 2007. Starting with this year's edition, the DTIS conference will be held during the end of March or the beginning of April.

The area of interest for the IEEE DTIS conference deals with the Design, Technology and Test of electronic products, ranging from integrated circuits through multi-chip modules and printed circuit board to full Systems and Microsystems, as well as examining the methodologies and tools used in the design of such products.

The number of submitted papers has been very successful. We received 124 papers from 17 different countries. The three topic areas of these submitted papers are on Design (74%), Test (13%) and Technology (13%). From these 124 submissions, 44 papers have been accepted for oral presentation (35%) and an additional 24 papers have been accepted as posters (19%). As a result, a very nice program has been set up including:

- 2 invited keynote speakers on:
  - ✓ DFT and Verification implementations for Carrier Grade systems, which will be given by Dr. Hedi Touati from Nortel, Canada.
  - ✓ Physical Design Automation at Transistor Level, which will be given by Dr. Ricardo Reis from Universida de Federal do Rio Grande do Sul (UFRGS) – Brasil.
- 44 oral presentations distributed in two parallel tracks,
- 24 poster presentations distributed in 3 poster sessions,
- One special session with 5 papers on Carbon Nanotube Transistors: Characterization, Compact Modelling and Circuit Design, chaired by Cristell Maneux from IXL, France.

We hope the attendees will enjoy the technical program as well as the social aspect of the conference in the beautiful town of Tozeur.

The conference chairs would like to thank all of you: the authors who have submitted their research papers and the members of the program committee who have been working hard on the paper reviews. This conference is finally the result of a team effort from voluntary people who have willingly given their time and energy: the Organization Committee who have handled the overall coordination; the Technical Program Committee who made the reviews, and last but by no means least, the MSc and PhD students who gave their valuable help in every organizing step.

We look forward to meet you in Tunisia during the IEEE DTIS'08 Conference and we hope that you will enjoy your stay.

M. Masmoudi & M. Renovell
General co-Chairs

C. Landrault & S. Ben Saoud
Program co-Chairs

General Conference Information

Conference location:

The 3rd IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era (IEEE DTIS'08) will be held at the Dar Cherait Hotel in Tozeur, Tunisia.

Hotel name: Dar Cherait Hotel *****

Conference Hotel web site: http://www.darcherait.com.tn/

Flight information:

Inside Tunisia, the internal flights are hosted by the company Sevenair.

During the week of 23 to 29 March 2008, the flights are scheduled as follows:

Departures from Tunis-Carthage airport to Tozeur:
- Sunday, Monday and Friday at 21H40
- Tuesday at 18H35
- Saturday at 14H00

Departures from Tozeur to Tunis-Carthage:
- Monday, Tuesday and Saturday at 05H50
- Tuesday at 20H00
- Sunday at 14H00

For more information, you may contact Sevenair at (216) 71 94 2626.

Tunisia: The Host Country

Official language:

The official language in Tunisia is Arabic. The second language is French and is well spoken by almost all Tunisians. The third language, witch is taught at school until the Baccalaureate, is English.

Bank opening times:

Monday – Friday: 8:00 AM – 4:00 PM
Saturday, Sunday: closed
In most Hotels and other official places, there are possibilities to exchange money. In addition, in the Dar Cherait Hotel and in many other places in Tozeur, cash machines are also available to withdraw TND cash using major credit cards and bank cards.

Climate: The middle temperature in March is about 25 °C.

Time Zone: GMT + 2 (Summer time).

Electricity: 220V, 50 Hz.

Conference Contact

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- Conference web site: http://www.emc-lab.org/Conferences/DTIS2008

- Conference Registration desk:

Conference Registration desk will be indicated in the Dar Cherait Hotel.
The Conference Registration will begin on Tuesday, March 25th starting from 8 AM.

- Conference Social Event:

A Conference Social Event is planned on Thursday**,** March 27th starting at 2pm.

- Conference official language:

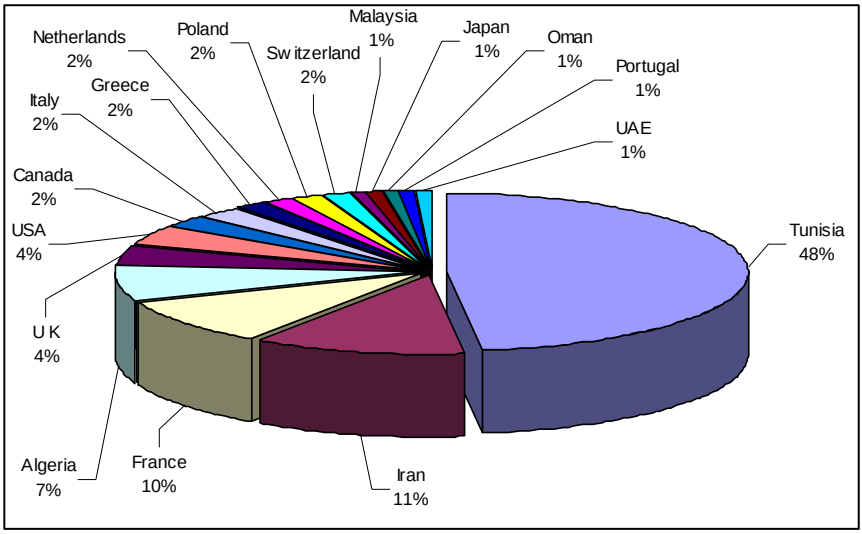
The official language of the Conference is English. It will be used in all presentations and all printed Conference materials.

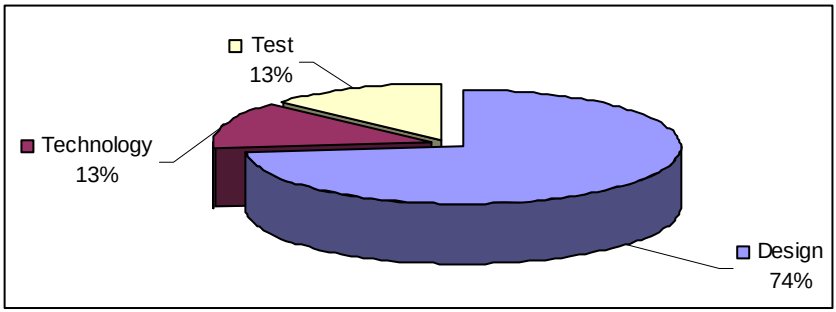
- Oral presentations:

A 25 min time slot (incl. discussion) is allocated for each Oral Presentation.
An LCD projector and a computer (MS Windows XP) with a CD-ROM drive, USB ports, and presentation software (MS PowerPoint, Adobe Acrobat Reader) will be available in both Conference rooms for Oral Presentations.

- **Maximum poster size:** (L=100cm) x (W=90cm).

Submitted papers Statistics





IEEE DTIS'08 Technical Program

Wednesday, March 26th 2008

08:00-09:00 REGISTRATION (Hotel Dar Cherait reception area)

09:00-10:00 OPENING SESSION (Room "CHEBBI" in the Museum entrance)

09:00-9:15 Welcome Address

M. Masmoudi – ENIS – Tunisia / **M. Renovell** – LIRMM – France
IEEE DTIS'08 General co-Chairs

09:15-09:30 Technical Program Introduction

C. Landrault – LIRMM – France / **S. Ben Saoud** – INSAT – Tunisia
IEEE DTIS'08 Program co-Chairs

09:30-10:00 Keynote

Title: DFT and Verification implementations for Carrier Grade systems

H. Touati – Nortel– Canada.

10:00-11:00 BREAK & POSTERS (Museum reception area)

10:00-11:00 Poster Session 1 (Museum reception area)

- **A Novel Relational Model based Hardware Simulator**; *H. Assasi, S. Mohammadi*; University of Tehran – Iran.
- **Signing Message Architecture Development Based on Open Source and Validation on a Software platform**; *W. Kaaniche, M. Masmoudi;* EMC-ENIS – Tunisia.
- **Design of a Transmission Gate based CMOS / Molecular (CMOL) Memory Cell**; *M. Barua, Z. Abid;* University of Western Ontario – Canada.
- **Current Conveyor Realization of Synchronized Chua's Circuits for Binary Communications;** *R. Trejo-Guerra, E. Tlelo-Cuautle, C. Cruz-Hernández, C. Sánchez-López, M. Fakhfakh***;** LETI-ENIS – Tunisia; INAOE-CICESE-UAT– Mexico.

- **Platform based design for a multimedia Motion JPEG decoder case study**; *A.C. Ammari, H. Harbegue, A. Jemai, K. Smiri;* INSAT-FST – Tunisia**.**
- **RF Transceiver Parameter Identification Using Regressive Models**; *R. Khereddine, E. Simeu, S. Mir*; TIMA laboratory – France.
- **VHDL-AMS Modelling of Current Convoyer cell for integration in RF-application**; *E. Gaddour Sallem, A. Fakhfakh, L. Kammoun;* LETI-ENIS – Tunisia.
- **A Programmable 6 bit DAC of current-Steering dedicated to nerve stimulator**; *N. Rekik, S. S'habou, A. Benhamida, M. Samet*; LETI-ENIS – Tunisia.
- **Use of Mini Heat Pipes For The Thermal Management of High Dissipative Electronic Packages**; *M.C. Zaghdoudi, S. Maalej, C. Tantolin, C. Sarno;* INSAT – Tunisia; DSI – France.

11:00-12:30 Panel (Room "CHEBBI")

Microelectronics Infrastructures for Education and Research: what is still missing?

Moderator: B. Courtois – CMP – France**.**

Panelists:

- **O. BONNAUD** – CNFM – France
- **B. COURTOIS** – CMP –France
- **W. MAROUFI** – SAGEM – Tunisia
- **L. SALAGER** – STMicroelectronics – Tunisia

12:30-14:00 LUNCH

14:00-15:40 SESSION 1

14:00-15:40 Session 1A: RF Design and Wireless 1 (Room "petit BEY")

Chairs: **H. Lapuyade** – IMS – France
M. Fakhfakh – LETI – Tunisia

- **A Linear wide Range Varactor**; *M.S. Jalali, N. Masoumi;* University of Tehran – Iran.
- **A Dual Wideband CMOS LNA design for The 4G of Wireless applications**; *M. Ben Amor, M. Loulou, S. Quintanel, D. Pasquet;* ENIS – Tunisia; ECIME – France.
- **A 863-870-Mhz Spread-Spectrum FSK Transceiver Design for Wireless Sensor**; *H. Trabelsi, G. Bouzid, F. Derbel, M. Masmoudi;* EMC-ENIS – Tunisia.
- **Pseudorandom Clock Signal Generation for Data Conversion in a Multistandard Receiver**; *M. Ben-Romdhane, C. Rebai, A. Ghazel, P. Desgreys, P. Loumeau;* SUP'COM – Tunisia; LTCI Telecom – France.

14:00-15:40 Session 1B: New components 1 (Room "ANDALOUSIA")

Chairs: **U. Schwalke** – ISTN – Germany
J.O. Klein – E. U. Inf. – France

- **A Nanoelectronic Array Structure based on two types of Molecular Switches**; *A. Alma'aitah, Z. Abid;* University of Western Ontario – Canada.

- **Inkjet printing of new photosensitive sensors based on organic thin films**; *T. Fiorido, M. Bendahan, K. Aguir, M. Barret, S. Sanaur, C. Martini, H. Brisset, C. Videlot-Ackermann, J. Ackermann, F. Fages;* L2MP – France.

15:40-16:40 BREAK & POSTERS (Dar Cherait pool area)

15:40-16:40 Poster Session 2 (Dar Cherait pool area)

- **Efficient Computation of Logic Circuits Reliability Based on Probabilistic Transfer Matrix**; *L. Alves de Barros Naviner, M. Correia de Vasconcelos, D. Teixeira Franco, J-F. Naviner;* GET/ENST-CNRS/LTCI – France.

- **Interconnect Sizing and Spacing with Consideration of Buffer Insertion for Simultaneous Crosstalk-Delay Optimization**; *F. Hasani, N. Masoumi*; Tehran University – Iran.

- **Reconfigurable Hardware Implementation of a Random Number Generator Based On 2-D Cellular Automata**; *Z. Guitouni, M. Machhout, R. Tourki*; FSM – Tunisia.

- **Adaptive motion estimator for the H264 coder**; *S. Dhahri, A. Zitouni, M. Hajji, R. Tourki;* FSM – Tunisia.

- **A Low-distortion Transconductance Amplifier;** *M. Mathew, K. Hayatleh, B.L. Hart, F.J. Lidgey;* Oxford Brookes University – United Kingdom.

- **Current Mode Pipelined A/D Converter;** *K. Wawryn, R. Suszynski, B. Strzeszewski;* Koszalin University of Technology – Poland.

- **Accurate Analysis of RF Noise Characteristics in Active MOSFET Mixers with 90 nm Technology**; *D. Fathi, N. Masoumi*; Tehran University – Iran.

- **LT-PRPG: Power Minimisation Technique for Test-per-Scan BIST**; *A.S. Abu-Issa, S.F. Quigley;* University of Birmingham – United Kingdom.

- **Comparative study and design of new low voltage high performance current mirrors**; *H. Bdiri Gabbouj, N. Hassen, K. Besbes;* FSM – Tunisia.

16:40-18:20 SESSION 2

16:40-18:20 Session 2A: Interconnect (Room "petit BEY")

Chairs: **R. Reis** – UFRGS – Brasil
M. Renovell – LIRMM – France

- **A New Approach of Coding to Improve Speed and Noise Tolerance of On-chip Busses**; *S. Pillement, O. Sentieys, JM Philippe;* University of Rennes 1 – France.
- **Crosstalk pulsewidth calculation**; *J.E. Lorival, D. Deschacht;* LIRMM-UM2 – France.
- **New Directions in Interconnect Performance Optimization**; *A. Courtay, J. Laurent, N. Julien, O. Sentieys;* University of South Brittany- University of Rennes 1 – France.
- **No Equidistance Buffer Insertion in Global Interconnect using Simulated Annealing**; *A. Amirabadi, N. Masoumi;* University of Tehran – Iran.

16:40-18:20 Session 2B: Low power (Room "ANDALOUSIA")

Chairs: **U. Schwalke** – ISTN – Germany
E. Simeu – TIMA – France

- **Very Low-Cost CMOS Audio Amplifier for 1-V Portable Applications**; *C. Azzolini, A. Ricciardi, A. Boni;* University of Parma – Italy.
- **A Low Power Baseband Processor for a Dual Mode UHF EPC Gen 2 RFID Tag**; *V. Roostaie, V.Najafi, S. Mohammadi, A. Fotowat-Ahmady;* KavoshCom R&D Group – Iran.
- **Peak Power Reduction Method for Between-Core Vector Overlapping Testing;** *W. Suzuki, T. Shinogi, T. Hayashi, H. Kawanaka, S. Tsuruoka;* Mie University – Japan.

Thursday, March 27th 2008

08:00-09:00 REGISTRATION

09:00-09:30 Invited Talk (Room "ANDALOUSIA")

Title: Physical Design Automation at Transistor Level

R. Reis – Universidade Federal do Rio Grande do Sul (UFRGS) – Brasil.

09:30-10:45 SESSION 3

09:30-10:45 Session 3A: Analog Design 1 (Room "petit BEY")

Chairs: **H. Lapuyade** – IMS – France
B. Courtois – CMP – France

- **Optimization of a rail to rail low voltage CCII for active filter applications**; *N. Bouaziz Elfeki, S. Ben Salem, D. Sellami Masmoudi, N. Derbel;* CIELS,LETI-ENIS – Tunisia.
- **Integrated Lock-In Amplifier for Contactless Interface to Magnetically Stimulated Mechanical Resonators**; *C. Azzolini, A. Magnanini, M. Tonelli, G. Chiorboli, C. Morandi;* University of Parma – Italy.

- **Optimizing CMOS Operational Transconductance Amplifiers through Heuristic programming**; *H. Daoud, S. Bennour, M. Fakhfakh, M. Loulou;* LETI-ENIS – Tunisia.

09:30-10:45 Session 3B: BIST (Room "ANDALOUSIA")

Chairs: **H. Aziza** – Polytech Marseille – France
M. Renovell – LIRMM – France

- **An Efficient ARchitecture for Accumulator-BAsed Test Generation of SIC pairs**; *I. Voyiatzis, C. Efstathiou;* TEI of Athens, University of Central Greece – Greece.
- **A Multi-Output Technique for High Fault Coverage in Test-Per-Scan BIST**; *Abdallatif S. Abu-Issa, Steven F. Quigley;* University of Birmingham – United Kingdom.
- **On Reducing Aliasing in Accumulator-Based Compaction**; *I. Voyiatzis;* TEI of Athens – Greece.

10:45-11:15 Coffee Break (Dar Cherait pool area)

11:15-12:30 SESSION 4

11:15-12:30 Session 4A: Analog Design 2 (Room "petit BEY")

Chairs: **H. Aziza** – Polytech Marseille – France
H. Lapuyade – IMS – France

- **A single rail DC voltage-to-current-converter**; *B. L .Hart, K Hayatleh, F. J. Lidgey;* Oxford Brookes University – United Kingdom.
- **Low Power Design of A Decimation Filter in Multi-Standard Receiver;** *N. Khouja, K. Grati, A. Ghazel, B. Le Gall;* CIRTA'COM Laboratory – Tunisia**;** IMS-Laboratory-Bordeaux 1 – France.
- **High Precision Time-to-Amplitude Converter for Diffuse Optical Tomography Applications**; *M. Kanoun, Y.B. Lauzière, R. Fontaine;* University of Sherbrooke – Canada.

11:15-12:30 Session 4B: Memory Design and Test (Room "ANDALOUSIA")

Chairs: **S. Hamdioui** – TuDelft – Netherlands
P. Girard – LIRMM – France

- **A Proven Qualification Methodology for Embedded CMOS Memory Compilers**; *R. Capraro, L. Ben Ammar;* ATMEL Rousset – France.
- **An Efficient Diagnosis Methodology for Charge Pump Circuits: Application to Flash EEPROM devices;** *H. Aziza, J-M. Portal, O. Ginez, E. Bergeret;* University of Marseille, ST Microelectronics – France
- **A Signature-based Approach for Diagnosis of Dynamic Faults in SRAMs**; *A. Ney, A. Bosio, L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel;* LIRMM – France.

12:30-14:00 LUNCH

14:00-00:00 Social event – Sight seeing & Special Dinner.

Friday, March 28th, 2008

08:30-09:45 Special Session: Carbon Nanotube Transistors: Characterization, Compact Modelling and Circuit Design (Room "petit BEY")

Chair**: C. Maneux** – IMS**,** University of Bordeaux I – France**.**

- **Structural and electrical characterization of carbon nanotube field-effect transistors fabricated by novel self-aligned growth method;** *L. Rispal, U. Schwalke*; Institute for semiconductor Technology and Nanoelectronics, Darmstadt – Germany.
- **Towards Compact Modelling of Schottky Barrier CNTFET**; *M. Najari, S. Frégonèse, C. Maneux, T. Zimmer, H. Mnif, N. Masmoudi*; IMS Bordeaux – France; LETI – Tunisia.
- **A Charge Approach for a Compact Model of Dual Gate CNTFET**; *J. Goguet, S. Frégonèse, C. Maneux, T. Zimmer*; IMS Bordeaux – France.
- **Mixed analog-digital design of a learning nano-circuit for neuronal architectures;** *M. Hé, J-O. Klein, E. Belhaire;* IEF Orsay – France.
- **Dynamically Reconfigurable Logic Gate Cells and Matrices using CNTFETs**; *I. O'Connor, J. Liu, D. Navarro, F. Gaffiot*; Lyon Institute of Nanotechnology – France.

09:45-11:00 SESSION 5

09:45-11:00 Session 5A: Analog Design 3 (Room "petit BEY")

Chairs: **H. Mnif** – LETI – Tunisia
P. Girard – LIRMM – France

- **Multistandard Digital Channel Selection Using Decimation Filtering for Delta Sigma Modulator**; *C. Rebai, S. Bourbia, N. Jouida;* SUP'COM – Tunisia.
- **Top-Down Design Process for Continuous-Time Delta Sigma Modulators**; *N. Jouida, C. Rebai, A. Ghazel, D. Dallet;* SUP'COM, Tunisia; ENSEIRB Bordeaux – France.
- **Design of Efficient Digital Interpolation Filters and Sigma-Delta Modulator for Audio DAC**; *N. Ben Ameur, M. Loulou;* LETI-ENIS – Tunisia.

09:45-11:00 Session 5B: Test and verification (Room "ANDALOUSIA")

Chairs: **C. Landrault** – LIRMM – France
H. Touati – NORTEL – Canada

- **Test structure generation to quantify filling impact**; *L. Remy, JM. Portal, P. Coll, F. Picot, P. Mico;* ATMEL Rousset-L2MP Marseille – France.

- **Formal proof between two designs having different level of abstraction**; *A. Maalej, P-Y. Martinez;* ST Microelectronics – Tunisia.

- **Adaptation of High Level Behavioral Models for Stuck-at Coverage Analysis**; *M. Zolfy, Z. Navabi, Z.D. Kozekanani;* Tabriz University – Iran.

11:00-11:45 BREAK & POSTERS (Dar Cherait pool area)

11:00-11:45 Poster Session 3 (Dar Cherait pool area)

- **Neural Network Based Edge Detection with Pulse Mode Operations and Floating Point Format Precision;** *A. Damak, M. Krid, D. S. Masmoudi;* CIELS-ENIS – Tunisia.

- **Dependability Consequences of Fault-Tolerant Technique Integrated in Stack Processor Emulator using Information Flow Approach**; *M. Jallouli, H. Belhadaoui, C. Diou, F. Monteiro, O. Malasse, J-F. Aubry, A. Dandache, G. Buchheit, H. Medromi;* LICM, Metz – France.

- **Obstacle Avoidance of a Mobile Robot Using a Hierarchical Control**; *C. Abdelmoula, M. Masmoudi, F. Chaari;* EMC-ENIS – Tunisia.

- **Topology-oriented System Design Exploration for Embedded Applications implemented onto Heterogeneous Multiprocessor SoC**; *F. Graziosi, L. Pomante, L. Imbriglio;* DEWS – Italy.

- **The Effect of Substrate Noise on a 5.2 GHz LC-Tank VCO Performance in a Lightly Doped Substrate;** *S. Aghnoot, N. Masoumi;* University of Tehran – Iran.

- **A Neural Controller for lane/wall following system**; *W. Makni, M.S. Masmoudi, M. Masmoudi, N. Derbel;* EMC-ENIS – Tunisia.

11:45-13:00 SESSION 6

11:45-13:00 Session 6A: Digital Design (Room "petit BEY")

Chair: **C. Landrault** – LIRMM – France

I. Voyiatzis – TEIA – Greece

- **FPGA Implementation of FHSS-FSK Modulator**; *G. Bouzid, H. Trabelsi, Z. Elabed, M. Masmoudi;* EMC-ENIS – Tunisia.

- **Efficient Hardware Architecture of Recursive Karatsuba-Ofman Multiplier**; *W. El Hadj Youssef, M. Zeghid, M. Machhout, B. Bouallegue, R. Tourki;* FSM – Tunisia; LESTER Lorient – France.

- **Implementation of JPEG 2000 MQ-Coder**; *T. Saidani, M. Atri, R. Tourki;* FSM – Tunisia.

11:45-13:00 Session 6B: New components 2 (Room "ANDALOUSIA")

Chairs: **M. Masmoudi** – ENIS – Tunisia
S. Ben Saoud – INSAT – Tunisia

- **Design and Implementation of a 3-DOF Optical Precision Sensor Integrated in Micro-Robots**; *N. Dave, F. Abdelkefi, J-M. Breguet;* EPFL – Switzerland.
- **MEMS-based reconfigurable Antenna for Enhanced GNSS localization;** *L. Petit, J. Ayadi;* CSEM – Switzerland**.**
- **A Spice Model for Single Electron Transistor Applications at Low Temperatures: inverter and ring oscillator**; *A. Boubaker, M. Troudi, N. Sghaier, A. Souifi, N. Baboux, A. Kalboussi;* INSA Lyon France; FSM – Tunisia.

13:00-14:30 LUNCH

14:30-16:10 SESSION 7

14:30-16:10 Session 7A: RF Design and Wireless 2 (Room "petit BEY")

Chairs: **A. Fakhfakh** – LETI – Tunisia
M. Renovell – LIRMM – France

- **Design optimization methodology of CMOS direct Down-conversion Mixer for Wireless Sensors**; *H. Thabet, M. Masmoudi;* EMC-ENIS – Tunisia.
- **Concepts and Optimization of CMOS LC-VCO Circuits via Geometric Program**; *D. Ben Issa, A. Kachouri, M. Samet;* LETI/ENIS – Tunisia.
- **Analysis and Design of 20 GHz VCOs using cross-coupled differential pair and Balanced Colpitts Topologies in SiGe:C BiCMOS Technology**; *J. Verdier, J. Cruz Nunez Perez, C. Gontrand;* Institute of Nanotechnologies of Lyon – France.

14:30-16:10 Session 7B: High level Design & Real Time systems

(Room "ANDALOUSIA")

Chairs: **S. Pillement** – IRISA – France
S. Ben Saoud – INSAT – Tunisia

- **Integration of a STBus Type 3 protocol custom component into a HLS tool**; *T. Tayachi, P-Y. Martinez;* ST Microelectronics – Tunisia.
- **Automated Macromodel Generation for High Level Modeling**; *L. Xia, I.M. Bell, A.J. Wilkinson,* University of Hull – UK.
- **FPGA HardCore Single Processor Implementation of RT Control Applications**; *S. Ben Othman, M. Ghrissi, A.K. Ben Salem, S. Ben Saoud;* INSAT – Tunisia.
- **RTOS for SoC Embedded Control Applications;** *A.K. Ben Salem, S. Ben Othman, H. Abdelkrim, S. Ben Saoud;* INSAT – Tunisia.

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